REMARKS

This Amendment responds to the Office Action dated August 16, 2010 in which the Examiner objected to claim 1 and rejected claims 1-50 under 35 U.S.C. § 103.

As indicated above, a minor informality in claim 1 has been corrected. Therefore, Applicant respectfully requests the Examiner withdraws the objection to claim 1.

As indicated above, claims 1, 2, 8, 10-12, 18, 20-21, 31 and 41 have been amended in order to make explicit what is implicit in the claims. The amendment is unrelated to a statutory requirement for patentability.

Claims 1-2, 8, 10, 21 and 31 claim a multiplexing apparatus and claims 11-12, 18, 20 and 41 claim a multiplexing method. The multiplexing apparatus and method multiplex base-band audio and video data using a stored instruction set which states the unit storage location, number of bytes and order of multiplexing. The claimed invention thus provides a multiplexing apparatus and method which reduces the processing burden on a CPU since the CPU does not have to transfer an instruction directly to a multiplexer at the time of transfer, but instead, the multiplex stream is generated by the multiplexer reading the instruction set from the memory. The prior art does not show, teach or suggest the invention as claimed in claims 1-2, 8, 10-12, 18, 20-21, 31 and 41.

Claims 1-3, 7, 11-13, 17, 21-23, 27, 31-33, 37, 41-43 and 47 were rejected under 35 U.S.C. § 103 as being unpatentable over *Robinett, et al.* (U.S. Publication No. 2002/0126711) in view of *Stein, et al.* (U.S. Publication No. 2003/0140212).

Robinett, et al. appears to disclose an audio-video program as composed of one or more coded bit streams or elementary streams (ES). Each ES is separately encoded. The encoded ESs are then combined into a systems layer stream such as a program stream PS or a transport

streams TS [0014]. *Robinett, et al.* is illustrated for TSs [0017]. Often it is desired to remultiplex TSs. Remultiplexing involves the selective modification of the content of a TS, such as adding transport packets to a TS, deleting transport packets from a TS, rearranging the order of transport packets in a TS and/or modifying the data contained in the transport packets [0025]. It is the object of *Robinett, et al.* to provide a flexible remultiplexing architecture [0027]. An illustrative application of *Robinett, et al.* is the remultiplexing one or more MPEG-2 compliant transport streams (TSs). TSs are bit streams that contain the data of one or more compressed/encoded audio-video programs [0033].

Thus, *Robinett, et al.* is merely directed to remultiplexing a transport stream (TS) (*i.e.* receiving a transport stream and thereafter remultiplexing the transport stream). However, as claimed in claims 1, 2, 8, 10-12, 18, 20-21, 31 and 41, the present invention is directed to multiplexing base-band video data from a video source and base-band audio data from an audio source (*i.e.* receiving base-band video and base-band audio). However, *Robinett, et al.* remultiplexes a transport stream (*i.e. Robinett, et al.* would be applied to the output of the present invention). Thus, *Robinett, et al.* is not a proper reference.

Additionally, *Robinett, et al.* merely discloses a remultiplexer node is provided with one or more adapters, each adapter including a cache, a data link control circuit connected to the cache and a direct memory access circuit connected to the cache. The data link control circuit has an input port for receiving transport streams and an output port for transmitting transport streams. Using an asynchronous communication link, the direct memory access circuit can access a memory in the remultiplexer node. The memory can store one or more queues of descriptor storage locations such as a queue assigned to an input port and a queue assigned to an output port. The memory can also store transport packets in transport packet storage locations to

which descriptors stored in such descriptor storage locations of each queue point [0034, emphasis added]. When an adaptor is used to input transport streams, the data link control circuit allocates to each received transport packet to be retained, an unused descriptor in one of a sequence of descriptor storage locations, of a queue allocated to the input port [0035, emphasis added]. When an adaptor is used to output transport packets, the data link control circuit retrieves from the cash each descriptor of a sequence of descriptor storage locations of a queue assigned to the output port. The descriptors are retrieved from the beginning of the sequence in order. The data link control circuit also retrieves from the cache the transport packets stored in the transport packet storage locations to which the descriptors point [0036, emphasis added]. Each descriptor is also used to restore a receipt time stamped indicating the transport packet is received that the input port or a dispatched time stamp indicating the time at which the transport packet is to be transmitted from the output port [0037, emphasis added]. The DMA control circuit 116 is for transferring transport packet data and descriptor data between the host memory 120 and the cache 114 [0076].

Thus, *Robinett, et al.* merely discloses a control circuit 116 for transferring transport packet data and descriptor data between the host memory and the cache 114. Nothing in *Robinett, et al.* shows, teaches or suggests (1) calculating an order of multiplexing based on storage location of audio/video data units, (2) generating a multiplexing instruction set of (a) a unit storage location, (b) number of bytes and (c) order of multiplexing and (3) storing the unit storage location, number of bytes and order of multiplexing as the multiplexing instruction set as claimed in claims 1, 2, 11, 12, 21, 31 and 41. Rather, *Robinett, et al.* only discloses a remultiplexer having a control circuit for transferring transport packet data and descriptor data between a host memory and a cache.

Stein, et al. appears to disclose a single instruction multiple data (SIMD) model assumes a plurality of processing cells. Each cell may include various combinations of hardware: address generator, multipliers, arithmetic logic units (ALUs), memory, registers, and sequencers [0003]. A single instruction multiple data (SIMD) array cell processes a data stream, the array including a plurality of cells, each cell includes a memory circuit for storing a predetermined region of the data stream, a location register circuit for representing the size and location of the predetermined region of the data stream, a unique identification number stored in its ID register circuit and an arithmetic logic unit responsive to the identification number and a single command common to all cells in a load mode to compute a unique start position for its cell for receiving the predetermined region of the data stream [0014]. The location register circuit may store a start position for the predetermined region to be stored in its memory, the length of the direct memory access data stream to be stored, and at least one dimension of the data stream. The location register may store the vertical and horizontal dimensions of the data stream. The command word in the execution mode may establish the size and location of the predetermined region in the location register circuit. The command word may include an address field for address and locations in the predetermined region of interest in the memory circuit. The command word in the execution mode may include a data field for operating the arithmetic logic unit. The condition code register and arithmetic logic unit may respond to the unique identification number, the data field, to control the condition of the cell [0015].

Thus, *Stein, et al.* merely discloses a single instruction multiple data array cell. Nothing in *Stein, et al.* shows, teaches or suggests multiplexing a base-band video data from a video source and a base-band audio data from an audio source in order to form a transport stream as

claimed in claims 1, 2, 11, 12, 21, 31 and 41. Rather, *Stein, et al.* is directed to a single instruction multiple data array circuit for processing a data stream.

Additionally, *Stein, et al.* merely discloses that the SIMD array cell includes a location register circuit representing the size and location of a predetermined region of the data stream it may store, a start position for the predetermined region to be stored, the length of the direct memory access data stream to be stored and at least one dimension of the data stream. Thus, nothing in *Stein, et al.* shows, teaches or suggests (a) calculating an order of multiplexing based on storage location of audio/video data units, (b) generating a multiplexing instruction set of a unit storage location, number of bytes and order of multiplexing and (c) storing the unit storage location, number of bytes and order of multiplexing as the multiplexing instruction set as claimed in claims 1, 2, 11, 12, 21, 31 and 41. Rather, *Stein, et al.* merely discloses a location register circuit storing the start position for the predetermined region, the length of the stream to be stored and at least one dimension of the data stream.

A combination of *Robinett, et al.* and *Stein, et al.* would not be possible since *Robinett, et al.* is directed to remultiplexing a transport stream while *Stein, et al.* is directed to a single instruction multiple data array cell including a memory circuit, a location register, a ID register circuit and an arithmetic logic unit. Even assuming arguendo that the references could be combined, the combination would merely suggest a remultiplexer operating on a transport stream as taught by *Robinett, et al.* and a location register storing a start position for a predetermined region to be stored, a length of a direct memory access data stream to be stored and at least one dimension of the data stream as taught by *Stein, et al.* Thus, nothing in the combination of the references shows, teaches or suggests (1) receiving base-band video data from a video source and base-band audio data from an audio source in order to form a multiplexed stream, (2)

calculating an order of multiplexing based on storage location of audio/video data units, (3) generating a multiplexing instruction set including a unit storage location, number of bytes and order of multiplexing and (4) storing the unit storage location, number of bytes and order of multiplexing as the multiplexing instruction set as claimed in claims 1, 2, 11, 12, 21, 31 and 41. Therefore, Applicant respectfully requests the Examiner withdraws the rejection to claims 1-2, 11-12, 21, 31 and 41 under 35 U.S.C. § 103.

Claims 3, 7, 13, 17, 22-23, 27, 32-33, 37, 42-43 and 47 recite additional features. Applicant respectfully submits that claims 3, 7, 13, 17, 22-23, 27, 32-33, 37, 42-43 and 47 would not have been obvious over *Robinett, et al.* and *Stein, et al.* within the meaning of 35 U.S.C. § 103 at least for the reasons as set forth above. Therefore, Applicant respectfully requests the Examiner withdraws the rejection to claims 3, 7, 13, 17, 22-23, 27, 32-33, 37, 42-43 and 47 under 35 U.S.C. § 103.

Claims 4-6, 14-16, 24-26, 34-36 and 44-46 were rejected under 35 U.S.C. § 103 as being unpatentable over *Robinett, et al., Stein, et al.* in view of *Kelly, et al.* (U.S. Publication No. 2001/0036355).

Applicant respectfully traverses the Examiner's rejection of the claims under 35 U.S.C. § 103. The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, Applicant respectfully requests the Examiner withdraws the rejection to the claims and allows the claims to issue.

As discussed above, since nothing in the combination of *Robinett, et al.* and *Stein, et al.* shows, teaches or suggests the primary features as claimed in claims 1, 12, 21, 31 and 41 as discussed above, Applicant respectfully submits that the combination of the primary references with the secondary reference to *Kelly, et al.* would not overcome the deficiencies of the primary

references. Therefore, Applicant respectfully requests the Examiner withdraws the rejection to claims 4-6, 14-16, 24-26, 34-36 and 44-46 under 35 U.S.C. § 103.

Claims 8-9, 18-19, 28-29, 38-39 and 48-49 were rejected under 35 U.S.C. § 103 as being unpatentable over *Robinett, et al, Stein, et al.* and further in view of *Dobson, et al.* (U.S. Patent No. 6,188,703).

As discussed above, *Robinett, et al.* is directed to a remultiplexer which remultiplexes a transport stream while *Stein, et al.* is directed to a single instruction multiple data array cell. Thus, nothing in the references shows, teaches or suggests (1) receiving base-band video data from a video source and base-band audio data from an audio source in order to form a multiplexed stream, (2) calculating an order of multiplexing based on storage location of audio/video data units, (3) generating a multiplexing instruction set of a unit storage location, the number of bytes and order of multiplexing of each data unit and (4) storing the unit storage location, number of bytes and order of multiplexing into a memory as the multiplexing instruction set as claimed in claims 8 and 18.

Dobson, et al. appears to disclose a FIFO buffer 32 which signals a MUX microprocessor 22 when sufficient video data is in a buffer 32 (column 3, line 65-column 4, line 3). When a start code is detected, the value of the FIFO-fullness-counter 40 is latched into another counter called the start-code position counter 48. The start-code position counter 48 only counts down on compressed data FIFO read by the MUX 30 (column 4, lines 31-35).

Thus, *Dobson, et al.* merely discloses a buffer which signals a microprocessor 22 when sufficient video data is in a buffer. Nothing in *Dobson, et al.* shows, teaches or suggests (a) calculating an order of multiplexing based on storage locations, (b) generating an instruction set of (1) the unit storage location, (2) the number of bytes and (3) the order of multiplexing and (c)

storing the unit storage location, number of bytes and order of multiplexing into a memory for the instruction set as claimed in claims 8 and 18. Rather, *Dobson, et al.* only discloses a buffer 32 signaling a microprocessor when it is filled with sufficient data.

A combination of *Robinett, et al*, *Stein, et al.* and *Dobson, et al.* would merely suggest to remultiplex a transport stream as taught by *Robinett, et al.*., to have a SIMD array cell include a location register circuit storing a start position, length of a direct memory access data stream and at least one dimension of the data stream as taught by *Stein, et al.* and to signal when sufficient data is in a buffer as taught by *Dobson, et al.* Thus, nothing in the combination of the references shows, teaches or suggests (1) receiving base-band video data from a video source and base-band audio data from an audio source to form a multiplexed stream, (2) calculating an order of multiplexing based on storage location of audio/video data units, (3) generating a multiplexing instruction set of a unit storage location, number of bytes and order of multiplexing and (4) storing the unit storage location, number of bytes and order of multiplexing as the multiplexing instruction set as claimed in claims 8 and 18. Therefore, Applicant respectfully requests the Examiner withdraws the rejection to claims 8 and 18 under 35 U.S.C. § 103.

Claims 9, 19, 28-29, 38-39 and 48-49 recite additional features. Applicant respectfully submits that claims 9, 19, 28-29, 38-39 and 48-49 would not have been obvious within the meaning of 35 U.S.C. § 103 over *Robinett, et al., Stein, et al.* and *Dobson, et al.* at least for the reasons as set forth above. Therefore, Applicant respectfully requests the Examiner withdraws the rejection to claims 9, 19, 28-29, 38-39 and 48-49 under 35 U.S.C. § 103.

Claims 10, 20, 30, 40 and 50 were rejected under 35 U.S.C. § 103 as being unpatentable over *Robinett, et al., Stein, et al.* in view of *Zaun, et al.* (U.S. Publication No. 2001/0024456).

As discussed above, *Robinett, et al.* is only directed to a remultiplexer remultiplexing a transport stream. Furthermore, *Stein, et al.* merely discloses a single instruction multiple data array cell including a location register circuit storing a start position for a region to be stored, a length of a direct memory access data stream and at least one dimension of the data stream. Nothing in *Robinett, et al.* and *Stein, et al.* show, teach or suggest (1) receiving base-band video data and base-band audio data to form a multiplexed stream, (2) calculating an order of multiplexing based on storage location of video/audio data units, (3) generating a multiplexing instruction set of a unit storage location, number of bytes and order of multiplexing and (4) storing the unit storage location, number of bytes and order of multiplexing as the multiplexing instruction set as claimed in claims 10 and 20.

Zaun, et al. appears to disclose a remultiplexing module including an output processor 124 which generates two or more output streams from data stored in packet buffers 104. The output processing section then generates two or more independent high-speed transport multiplex output streams incorporating the selected packet data [0035].

Thus, *Zaun, et al.* merely discloses a remultiplexing module outputting two or more multiplexed streams. Nothing in *Zaun, et al.* shows, teaches or suggests (a) calculating an order of multiplexing based on storage location of audio/video data units, (b) generating an instruction set of a unit storage location, number of bytes, order of multiplexing and type of multiplexed stream and (c) storing the unit storage location, number of bytes, order of multiplexing and type of multiplexed stream into a memory as the instruction set as claimed in claims 10 and 20. Rather, *Zaun, et al.* merely discloses a remultiplexing module outputting two or more multiplexed streams.

A combination of *Robinett, et al.*, *Stein, et al.* and *Zaun, et al.* would merely suggest to remultiplexing a transport stream as taught by *Robinett, et al.*, to have a single instruction multiple data array cell include a location register circuit storing a start position of a predetermined region to be stored, the length of the direct memory access data stream to be stored and at least one dimension of the data stream as taught by *Stein, et al.* and to output two or more multiplexed streams by a remultiplexing module as taught by *Zaun, et al.* Thus, nothing in the combination of the references shows, teaches or suggests (1) receiving base-band video data from a video source and base-band audio data from an audio source to form a multiplex stream, (2) calculating an order of multiplexing based on storage location of audio/video data units, (3) generating a multiplexing instruction set of a unit storage location, number of bytes and order of multiplexing and (4) storing the unit storage location, number of bytes and order of multiplexing as the multiplexing instruction set as claimed in claims 10 and 20. Therefore, Applicant respectfully requests the Examiner withdraws the rejection to claims 10 and 20 under 35 U.S.C. § 103.

Claims 30, 40 and 50 rec ite additional features. Applicant respectfully submits that claims 30, 40 and 50 would not have been obvious within the meaning of 35 U.S.C. § 103 over *Robinett, et al., Stein, et al.* and *Zaun, et al.* at least for the reasons as set forth above. Therefore, Applicant respectfully requests the Examiner withdraws the rejection to claims 30, 40 and 50 under 35 U.S.C. § 103.

Thus, it now appears that the application is in condition for a reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested. Should the Examiner find that the application is not now in condition for allowance, Applicant respectfully requests the Examiner enters this Amendment for purposes of appeal.

CONCLUSION

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is requested to contact, by telephone, the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicant respectfully petitions for an appropriate extension of time. The fees for such extension of time may be charged to Deposit Account No. 50-0320.

In the event that any additional fees are due with this paper, please charge to our Deposit Account No. 50-0320.

Respectfully submitted,

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Date: September 23, 2010

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